AMENDMENTS TO THE CLAIMS

PLEASE AMEND CLAIMS 1 to 15 AS FOLLOWS:

1. (Currently amended) A method of diagnosing a failure in a circuit in a complex semiconductor device ~~utilizing logic circuits, formed of latches, that have failed functional testing~~ comprising the steps of:

selecting a semiconductor device having logic circuits formed of latches;

testing the logic circuits in the device and locating a failing logic circuit in said device;

selecting a functional test procedure;

selecting a structural design and test technique;

combining said ~~with~~ functional test procedure and said structural design and test ~~techniques~~ technique to dynamically create a new test pattern based on the ~~functional~~ located failure; and

diagnosing the failing circuit to ~~determining~~ determine the location ~~of~~ and type of error in the said failing circuit.

2. (Currently amended) The method of claim 1, wherein the step of said combining functional testing of the device circuitry with structural design and test techniques to dynamically create a new test pattern based on the functional failure includes the step of transforming a functional pattern ~~into~~ into a scan deterministic pattern.

3. (Currently amended) The method of claim 2, wherein the failing logic circuit ~~device circuitry~~ is diagnosed as stuck at zero.

4. (Currently amended) The method of claim 2, wherein the failing logic circuit ~~device circuitry~~ is diagnosed as stuck at one.

5. (Currently amended) The method of claim 2, wherein the failed logic circuit ~~device circuitry has~~ is diagnosed as having AC faults.

6. (Currently amended) The method of claim 2, wherein the failed logic circuit ~~device circuitry has~~ is diagnosed as having transitional faults.

7. (Currently amended) A method of testing a complex semiconductor device by transforming a functional pattern into a scan determinative pattern ~~utilizing scan chains and logic circuits, formed of latches~~, consisting of the steps of:

selecting a first semiconductor device having a plurality of storage latches concatenated in a scan chain that includes embedded circuit memories;

performing a functional test, ~~comprised~~ consisting of a selected number of test cycles, on said semiconductor device;

identifying ~~any failure~~ a failing latch in a logic circuit in the scan chainduring the functional test;

unloading the values ofall the latches from the scan chain before the identified failing latch ~~failure may include reading the embedded circuit memories and other circuit storage elements~~;

generating a Load from the unloaded ~~states of the latches~~; values of all the latches from the scan chain before the identified failing latch;

selecting a second correctly operationg semiconductor device having a plurality of storage latches concatenated in a scan chain identical to said first device;

applying the generated Load ~~which~~ as the first event of ~~a newly created independent~~ an LSSD deterministic pattern by using the same identical primary inputs and Clocks that produced the failure ~~to~~ in said failing latch in said first semiconductor device to said second semiconductor ~~known~~ correctly operating device using a ~~the~~ bootstrapping technique;

and unloading the output of said second semiconductor device ~~the correctly operating device~~ to generate a deterministic LSSD pattern; and ~~operating~~ applying the generated deterministic LSSD pattern to the failing device and

diagnosing the failure using existing LSSD deterministic tools.

8. (Currently amended) The method of claim ~~3~~ 7, wherein said scan chain ~~chains are~~ is an LSSD scan chain ~~chains~~ and said created independent deterministic pattern is an ~~patterns are~~ LSSD deterministic ~~patterns.~~ pattern.

9. (Currently amended) The method of claim ~~3~~ 7, wherein said scan chain ~~chains are~~ is a GSD scan chain ~~chains~~ and said created independent deterministic pattern is a ~~patterns are~~ is a GSD deterministic ~~patterns.~~ pattern.

10. (Currently amended) A method of diagnosing a complex semiconductor device utilizing logic circuits, formed of latches, ~~that have failed functional testing~~ comprising the steps of:

subjecting a first semiconductor device, having embedded sequential logic circuits and storage circuits including a plurality of latches arranged in a LSSD scan chain to a test that consists of applying a plurality of primary inputs and clock signals to said device;

identifying a ~~failing vector of the~~ failed latch in a logic circuit in said scan chain during ~~functional~~ said test;

observing the states of the logic circuit containing said failed latch ~~device~~ by unloading the values of the plurality of latches from the LSSD scan chain positioned in said scan chain before the ~~failing vector~~ identified failed latch which may include reading any ~~the~~ embedded circuit memories and other circuit storage elements positioned in said scan chain before the failed latch

generating a LOAD from the unloaded states of the latches positioned in said scan chain before the failed latch;

applying the generated LOAD ~~which~~ as the first event of a newly created independent LSSD deterministic pattern by using ~~the same identical~~ primary inputs and Clocks signals identical to the primary inputs and clock signals that produced the failure to a known, correctly operating, device utilizing logic circuits formed of a plurality of latches arranged in a LSSD scan chain and a plurality of other storage

elements identical to said failed device by applying a plurality of primary inputs and clock signals to said device by using a ~~the~~ bootstrapping technique; ~~and~~

unloading the output of the correctly operating device to generate a deterministic LSSD pattern; ~~and~~

operating the generated deterministic LSSD pattern to the failing device; and

diagnosing the failure using existing LSSD deterministic tools.

11. (Currently amended) The method of claim ~~6~~ 10, wherein said scan chains are GSD scan chains and said created Independent deterministic patterns are GSD deterministic patterns.

12. (Canceled) A method of diagnosing a complex semiconductor device utilizing logic circuits, formed of latches, that have failed functional testing comprising the steps of:
combining functional testing of the device circuitry with structural design and test techniques to dynamically create new test patterns based on the functional failure; and
determining the location of and type of error in the failing circuit.

13. (Currently amended) The method of claim 1 wherein the step of said combining functional testing of the device circuitry with structural design and test techniques to dynamically create new test patterns based on the ~~functional~~ diagnosed failure includes the step of transforming functional patterns into scan deterministic patterns.

14. (Cancelled) A testing protocol for determining whether any of the internal functional circuit elements in a complex solid state device is stuck, comprising the steps of:

applying a predetermined set of functional vectors have been applied thus allowing functional patterns to a solid state device;

allowing the set of device run at speed until the failing point is reached:

unloading the data from said device state of the machine; and Isolating the fault.

15. (Currently amended) The testing protocol of claim 8 wherein the scan access ~~Initializes~~ initializes the internal state of the device prior to applying ~~the functional patterns~~ a predetermined set of functional vectors to narrow the partition of the functional patterns; and

iteratively executing multiple partitions to said set of functional vectors to ultimately yield one or more independent scan test vectors.